REMARKS

The present preliminary amendment is prepared in accordance with the new revised requirements of 37 C.F.R. § 1.121. A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

The present preliminary amendment is being filed concurrently with a Request for Continued Examination under 37 CFR 1.114 of the subject patent application.

The claims have been amended to clarify that the claimed method and module are directed to an electronic module that is assembled by attaching a chip to a substrate using a first solder interconnection array and attaching a board (e.g., and organic board) to the substrate using a second solder interconnection array such that a space is defined between the board and substrate. This space has a gap height ranging from about 300 microns to about 900 microns, whereby the second solder interconnection array resides entirely within this space. An underfill material is provided within the space prior to applying compressive forces to the electronic module. This underfill material may be applied only at discrete locations within this space. The underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns that is present in an amount ranging from about 60 to 64 weight percent.

An essential feature of the invention is that the underfill material is provided within the space between the board and the substrate *after* the board has been attached to the substrate but prior to applying compressive forces to the module. The underfill material is provided such that it is in direct contact with both the board and the substrate to maintain the space and optimize integrity of the second solder

interconnection array during application of compressive forces. The underfill is cured to form a rigid matrix within the space that maintains and enhances the integrity of the second solder interconnection array.

Applicants respectfully submit that the present claims are patentable over the prior art of record.

It is submitted that Jackson et al. (US Patent No. 6,333,563) teaches single melt solder alloy material interconnects 22 joined between a substrate 20 and organic interposer 30, and an underfill 24 of a low melt material filling the exposed area between the substrate 20 and the interposer 30. (Col. 3, ll. 6-41, and Fig. 2.) Attached to a bottom of the interposer 30 is another set of interconnect materials 32 having a higher melting temperature than underfill 24. (Col. 3, ll. 25-41.) The interposer is joined to an organic board 40 using the dual melt material 32. (Col. 3, ll. 42-57 and Fig. 4.) As recognized by the Examiner, Jackson does not teach providing an underfill material in the space between the circuit board and the substrate.

Peterson (US Patent No. 5,011,870) has been cited to overcome the deficiencies of Jackson. Applicants submit that Peterson does not disclose, contemplate or suggest underfill materials for use between a substrate and a board, whereby the underfill material is provided within the space between the board and the substrate *after* the board has been attached to the substrate such that the underfill directly contacts both the board and the substrate. In fact, as has also been recognized by the Examiner in the Advisory Action, the Examiner states that Peterson teaches the conventional "no-flow" underfill process in which the encapsulant is applied to the board before the electronic device is mounted, not after as is currently claimed. Further, Peterson does not disclose, contemplate or suggest that the encapsulant directly contacts both the board

and the substrate for maintaining the space therebetween and optimize the integrity of the second solder interconnection array therebetween, also as is claimed.

Applicants also continue to submit that the compositions of Peterson are different than those of the present invention.

Referring to Table 2 of Peterson, the encapsulant composition disclosed in Peterson contains 80 wt% of a filler mixture that comprises a first filler (e.g., AlN having an average particle size no larger than one micron) and a second filler (e.g., silicon metal having an average particle size of from 10 to 100 microns). The thermal conductivity is maximized when the weight ratio of the second filler to first filler is 1:1 and 4:1.

The 4:1 ratio comprises 64 wt% Si metal (particle size from 10 to 100 microns) to 16 wt% AlN (particle size no larger than one micron), while the 1:1 ratio comprises 40 wt% Si metal (particle size of from 10 to 100 microns) to 16 wt% AlN (particle size no larger than one micron).

However, this filler mixture is only 80 wt% of the entire encapsulant composition. As such, this would not equate to the entire encapsulant composition having 64 wt% Si metal to 16 wt% AlN, but rather 51.2 wt% (of a particle size from 10 to 100 microns) to 12.8 wt% of the entire encapsulant composition (i.e., underfill). (Col. 7, l. 30 to col. 8, l. 16.)

None of Peterson's encapsulant compositions with filler mixtures equate to an underfill material having a filler with a particle size from about 32-300 microns present in an amount ranging from about 60 to 64 wt% of the underfill, as is currently claimed.

Cui (US Patent No. 6,274,650) also does not dislcose or suggest an underfill material having the claimed particle sizes and weight percents between a substrate and a board, and as such, does not overcome the deficiencies of either Jackson et al. or Peterson.

As recognized by the Examiner, Kumamoto et al. (US Patent No. 6,632,704) discloses an underfill material having a filler material present in an amount ranging from about 80% by weight per solution, with the filler material having a particle size ranging from about 4 to 12 microns. Applicants submit that this is a difference in kind, not degree, such that Kumamoto does not rectify the deficiencies of any of the other cited prior art references, alone or in any proper combination thereof.

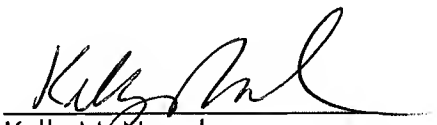
Morganelli et al. (US Patent No. 7,047,633) is cited for the limitation of providing a partial underfill material in an interconnection. However, applicants submit that Morganelli does not disclose, contemplate or suggest any of the above discussed deficiencies of the prior art, such that, this reference does not overcome the deficiencies of Jackson, Peterson, Cui, or Kumamoto, alone or in any proper combination thereof.

Applicants submit that the cited prior art references, in any proper combination thereof, do not render obvious the present invention.

In the light of the amendments to the claims it is believed that the present RCE application is in condition for allowance which action is respectfully solicited.

Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



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